What is claimed is:

1. A word line repair circuit in a flash memory device, comprising:

a main cell array in which a plurality of cell are classified in a I/O block unit;

a redundancy cell array consisting of repair blocks in which the number of word lines is equivalent to the number of columns constituting the I/O block and the number of cells connected to the word line is equivalent to the number of the I/O block;

a CAM cell array for storing information including information on a fail word line of the main cell array and connection information on the repair block instead of the fail word line;

a word line voltage switching unit for transferring a word line voltage applied to the fail word line to the redundancy cell array according to information on the fail word line; and

a word line select means enabled by the connection information, for selecting a word line of the repair block corresponding to a column of the I/O block according to the column select signal of the main cell array and then applying the word line voltage to the selected word line,

wherein data to be stored through the fail word line are sequentially stored through a corresponding column of the repair block in a I/O block unit, thereby repairing the fail word line.

2. The word line repair circuit as claimed in claim 1, wherein the I/O block is 16 in number.

3. The word line repair circuit as claimed in claim 1, wherein the I/O block consists of 1024 word lines and 64 columns and the repair block consists of 64 word lines and 16 columns.

4. The word line repair circuit as claimed in claim 1, wherein the word line voltage switching unit comprises:

first switching means each connected between the word line voltage supply terminal and the word line of the main cell array and driven by a fail word line signal of the CAM cell array;

an inverter for inverting the fail word line signal; and

a second switching means for transferring the word line voltage to the word line select means according to the fail word line inverted signal from the inverter.

5. The word line repair circuit as claimed in claim 4, wherein the first switching means and the second switching means are field effect transistors.

6. The word line repair circuit as claimed in claim 1, wherein the word line select means is provided every repair block.

7. The word line repair circuit as claimed in claim 1, wherein the word line select means comprises:

a first switching means driven by an enable signal depending on the connection information stored at the CAM cell array, for switching the word line voltage; and

a plurality of switching means each connected between the first switching means and the word line of the repair block, for switching the word line voltage to a word line of a repair block corresponding to a corresponding column according to the column select signal of the main cell array.